Fast solver to get steady-state waveforms for power converter design

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Abstract

Designing a power converter requires a good prediction of electrical quantities. Steady-state waveforms are needed but using a time-domain simulator to determine accurately these steady-state waveforms is generally too slow, so the designer usually uses a simplified analytical formulation to estimate these electrical quantities. This is not always accurate, must be repeated for each new circuit, and can be tedious for complex topologies. In this paper we show that a frequency-domain solver based on a Modified Nodal Analysis of the circuit can be used to obtain accurate results in little time even for a complex circuit, which makes it an efficient building block for a design tool. Accuracy and speed is demonstrated using comparisons with the steady-state analysis of Plecs® - which relies on a time-domain solver.

1. Introduction

Power converter design is an important challenge in the industrial field, but few software tools can really assist designers in the "operational" design step. The need for new tools has been clearly stated several times [1]. In a power converter design process, determining the main electrical variables (average, maximum and RMS values) and steady-state waveforms of the circuit is usually made by the designer with analytical formulas. This must be done for each new circuit and may require assumptions to simplify the description of complex topologies, which reduces the accuracy. Using a time-domain solver could increase the accuracy, but in a design process it may be used iteratively to explore the design space and the computation time multiplied by the number of iteration might be unacceptable. To face the issue, frequency modelling of power converter has been studied these last years to get electrical quantities in little time: [2] introduced a frequency solver to get steady-state waveforms of power converters based on commutation cells with hard switching and [3] studied the modeling of power converter topologies based on rectifier bridges.

Therefore, in this paper we detail the frequency solver adapted to commutation cells and based on the modified nodal analysis (MNA). It provides a generic method to get steady-state waveforms of power converters based on commutation cells with hard switching.

The first part of this paper deals with the principle of the proposed solver: a frequency solver adapted to the commutation cell.
The second part deals with the principle of the modified nodal analysis and frequency resolution used in the proposed solver.
The third part shows a performance evaluation of the proposed solver thanks to a comparison with the time-domain solver of the well-known simulation tool Plecs® [4].
At last, the fourth part deals with the use of the proposed solver in a computer-aided engineering platform dedicated to power converter design.

2. Principle of the frequency solver adapted to the commutation cell

The proposed frequency solver is based on the modified nodal analysis - described in section 3 - and adapted to the commutation cell which builds most of power converters.

2.1. Commutation cell model

To be used with the frequency solver, the commutation cell is modelled by a current source I_{HV} at high voltage side and a voltage source V_{LV} at low voltage side, forming two independent circuits as shown in Fig. 1.

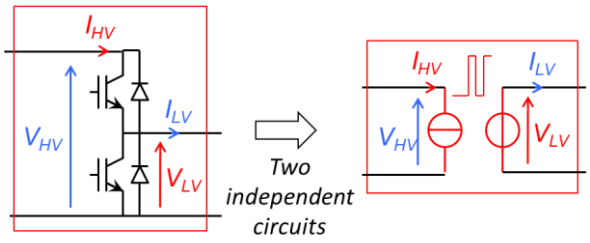


Fig. 1: Switching cell model

The values of current source I_{HV} and voltage source V_{LV} are analytically computed from:

$$V_{LV}(t) = D(t) \cdot V_{HV}(t)$$
$$I_{HV}(t) = D(t) \cdot I_{LV}(t) \quad (1)$$

Where $D(t)$ is the duty cycle of the commutation cell. Possible high frequency ripples in current I_{LV} and voltage V_{HV} are neglected to compute current I_{HV} and voltage V_{LV}.

2.2. Main process

To illustrate the main process, the circuit of a simple dc-dc chopper is considered in Fig. 2, using the commutation cell model.

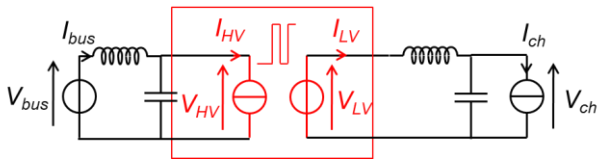


Fig. 2: Considered circuit with the commutation cell

The full process can be summarized with three steps shown in Fig. 3:

- Frequency spectrums of current I_{HV} and voltage V_{LV} are first obtained thanks to the Fast Fourier Transform (FFT) algorithm.
- Then, the MNA resolution is applied on all frequencies of the spectrum and the different voltages or currents of the circuits $(I_{LV}, V_{HV}, V_{ch}, I_{bus} \dots)$ are determined.
- At last, the Inverse Fast Fourier Transform (IFFT) algorithm can be used to derive the time-domain quantities at both sides of commutation cell.

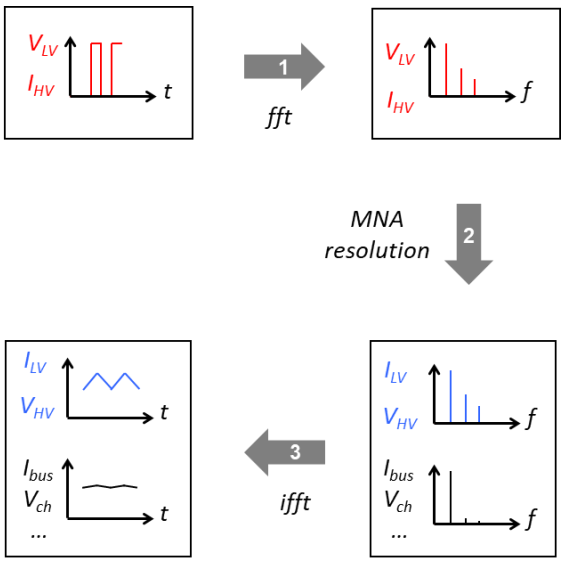
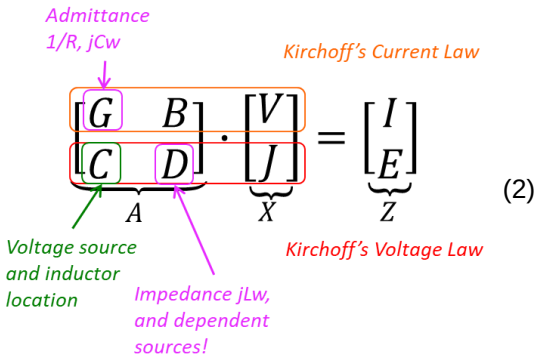


Fig. 3: Frequency resolution adapted to the commutation cell

3. Principle of the Modified Nodal Analysis and frequency resolution

3.1. Principle of the modified nodal analysis

The Modified Nodal Analysis [5] (MNA) is an equation formulation for circuits, which is based on Kirchoff's voltage and current laws. Spice [6], [7] is a well-known circuit simulator based on this MNA. MNA applied to a circuit with passive elements, independent current and voltage sources and active elements results in a matrix equation of the form $[A] \cdot [X] = [Z]$ such as:

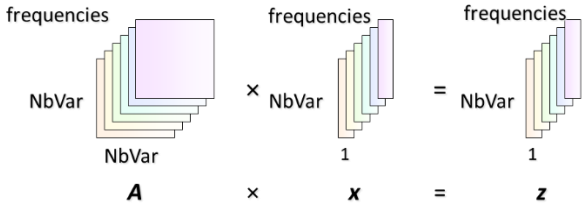


$$\begin{bmatrix} G & B \\ C & D \end{bmatrix} \cdot \begin{bmatrix} V \\ J \end{bmatrix} = \begin{bmatrix} I \\ E \end{bmatrix} \quad (2)$$

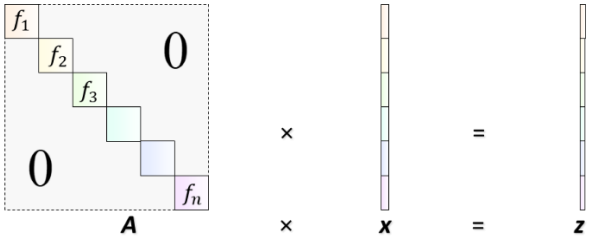
Where $[X]$ is a vector which holds the unknown quantities (node voltages *V* and currents *J*). Any linear equation system solver can solve this system for $[X]$.

3.2. Frequency resolution

The principle of this circuit resolution is adapted to power converter circuit: it is applied to the spectrum of the different voltages and currents of the circuit. Thus, the matrix system of (2) is built for each considered frequency as illustrated in Fig. 4(a), gathered as a single matrix as shown in in Fig. 4(b), and then solved. Therefore the $[x]$ vector holds the spectrums of the electrical quantities of the circuit.



(a)



(b)

Fig. 4: MNA Matrix system built for all considered frequency

4. Performance evaluation

4.1. Considered circuit

To evaluate the accuracy of this frequency resolution, a circuit composed of an inverter leg and a R-L-V load is considered and shown in Fig. 5.

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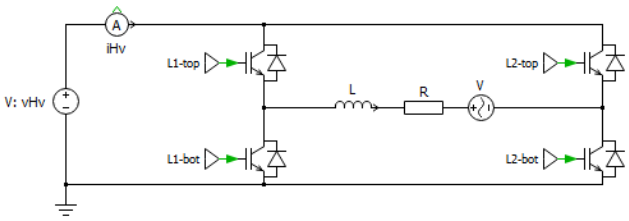


Fig. 5: Considered circuit composed of an inverter leg

The different parameter values used are shown in Table 1.

Parameter name	*Value*
V_{HV}	750 V
V_{RMS}	230 V
f	50 Hz
I_{RMS}	20 A
f_{sw}	2 kHz
L	5 mH
R	0.01 Ω

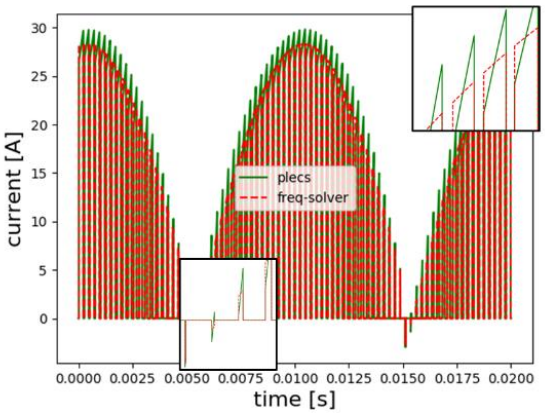
Table 1: Parameter values used

4.2. Results and comparison

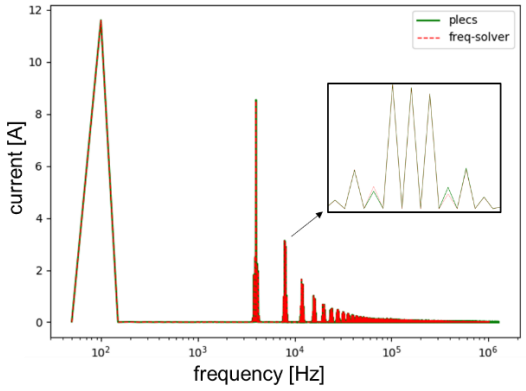
The results obtained with the proposed frequency solver are compared with the steady-state analysis of Plecs®. The frequency solver bandwidth is 1024 *kHz* and the time-domain solver uses a variable time-step. For this example, the Plecs® analysis ran in 6.1645 *s* and the frequency resolution in 0.404 *s*, more than 15 times faster.

Fig. 6 and Fig. 7 present waveform and spectrum comparisons of i_{HV} and i_{LV} currents for both solvers showing good matching As explained above in 2.1, the ripple of i_{LV} is neglected when determining the waveforms at the high-voltage side and we have a significant difference on the time domain waveform of current i_{HV} for example, as shown in the zoom of Fig. 6(a). However, differences of the spectrum of i_{HV} current in the frequency domain are very small as shown in Fig. 6(b). Table 2 shows the harmonic magnitudes of i_{HV} current obtained with Plecs® and the proposed

frequency solver with a maximum relative error of 1 %.
Yet, when it comes to filter design, accuracy in the frequency domain is certainly what matters, so this formulation offers a good accuracy / computation time ratio, i.e. a very good performance / cost ratio in the context of converter design.

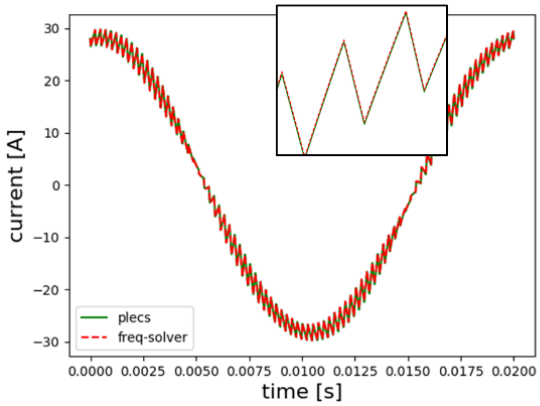


(a) Waveform of current i_{HV}

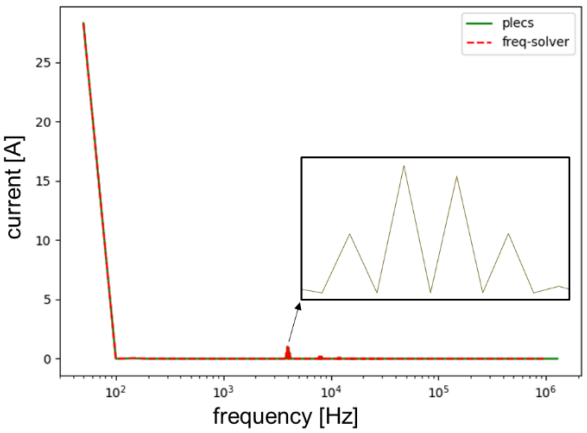


(b) Frequeny spectrum of current i_{HV}

Fig. 6: Waveform and spectrum of current i_{HV}



(a) Waveform of current i_{LV}



(b) Spectrum of current i_{LV}

Fig. 7: Waveform and spectrum of current i_{LV}

Frequency [Hz]	*Plecs®*	*Frequency solver*	*Relative error*
100	11.60	11.59	0.001
4 000	8.54	8.50	0.005
8 000	3.05	3.04	0.005
12 000	1.13	1.12	0.01

Table 2: Harmonic magnitudes of i_{HV} current: PLECS® and frequency solver

5. Application to a power converter design tool

The proposed solver is implemented in a computer-aided engineering platform dedicated to power converter design: Powerforge® [8]. This platform proposes to help users design power converters including multilevel topologies as a freedom degree. Main steps or the design process are given in 5.1.
Two conversion stage examples are then considered: a non-isolated dc-dc converter (Fig. 8) with specifications in Table 1Table 3 and a three-phase inverter (Fig. 9) with specifications in Table 4. For each conversion stage, the CPU time (on an Intel Core I5 1.6 GHz with 8 Go of RAM) needed to perform the design and the semiconductor losses will be highlighted.

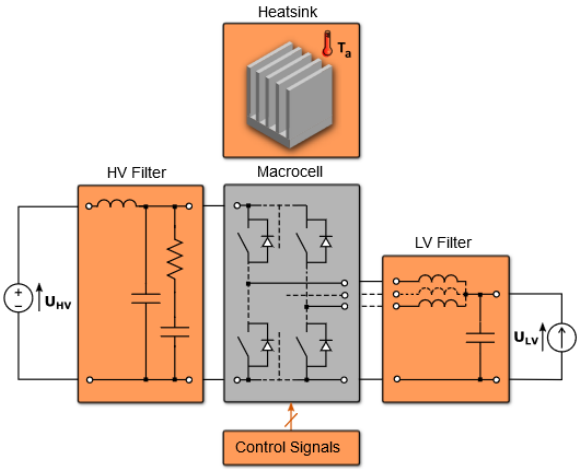


Fig. 8: Circuit of a multilevel non-isolated dc-dc converter

U_{HV}	540 V
U_{LV}	200 V
$P_{transfer}$	10 kW
f	10 kHz

Table 3: Specifications of the non-isolated dc-dc converter

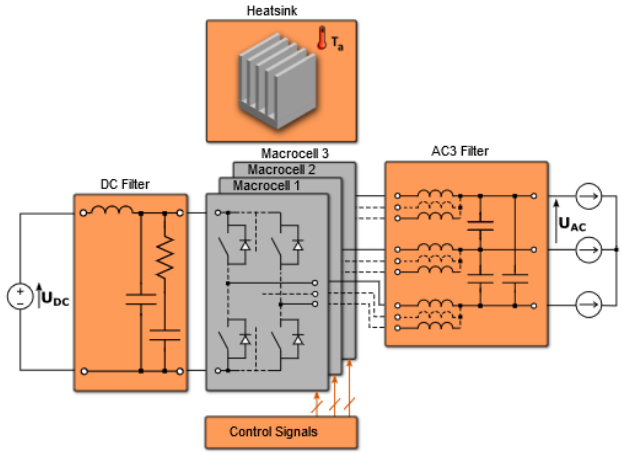


Fig. 9: Circuit of a multilevel three-phase inverter

U_{DC}	750 V
$U_{AC\ (RMS\ phase-phase)}$	380 V
$P_{transfer}$	10 kW
f_0	50 Hz
f_{sw}	10 kHz

Table 4: Specifications of the three-phase inverter

Semiconductor reference	*Topology*
SCT30N120	3-level, $n_{cell(par)} = 2$
SCT2160KE	5-level, $n_{cell(par)} = 4$
IKB20N60H3	7-level, $n_{cell(fc)} = 2$, $n_{cell(par)} = 3$

Table 5: Semiconductor references vs topology for the non-isolated dc-dc converter

For each conversion stage, three designs were performed with respectively three semiconductor references leading to three different topologies. These semiconductor references and topologies are presented in Table 6 and Table 7 respectively for the non-isolated dc-dc converter and the three-phase inverter.

Semiconductor reference	*Topology*
SCT30N120	3-level, $n_{cell(par)} = 2$
SCT2160KE	5-level, $n_{cell(par)} = 4$
IKB20N60H3	7-level, $n_{cell(fc)} = 2$, $n_{cell(par)} = 3$

Table 6: Semiconductor references vs topology for the non-isolated dc-dc converter

Semiconductor reference	*Topology*
C2M0045170D	2-level
C2M0040120D	3-level, $n_{cell(fc)} = 2$
SCT3080KL	3-level, $n_{cell(par)} = 2$,

Table 7: Semiconductor references vs topology for the three-phase inverter

5.1. Main steps of the design process

From specifications (voltage, power levels, ambient temperature, filtering requirements…) and user choices (semiconductor reference, switching frequency, materials), the main steps are presented in Fig. 10:

- Design of the multilevel switching cell: determination of the number of cells in parallel $n_{cell(par)}$ and of the number of cells in series $n_{cell(fc)}$ [9].
- Design of the filters
- Design of the cooling device
- Performance evaluation
  Constraint check (maximum junction temperature, filtering requirements…)

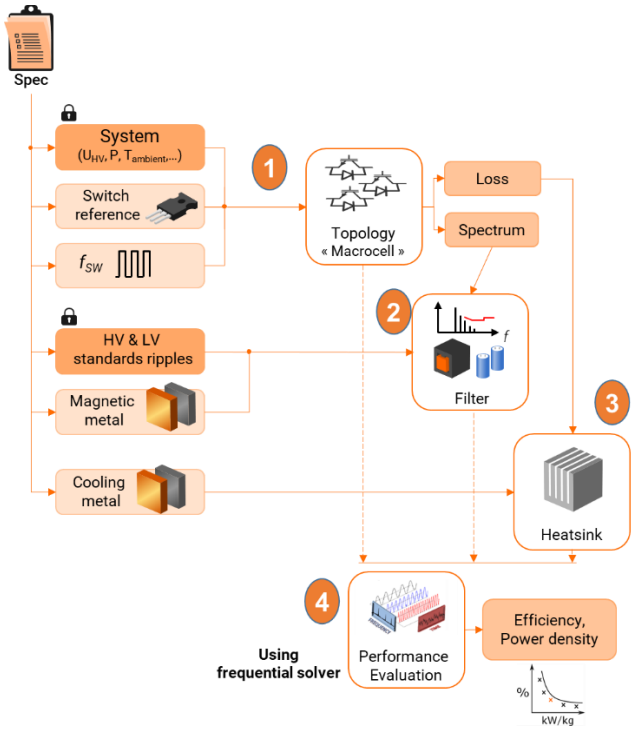


Fig. 10: Main steps of the design process

5.2. CPU time

Table 8 shows the different CPU time spent to design several multilevel topologies in the case of a non-isolated dc-dc converter. As these times are very short, it leaves room to explore different options to find the most relevant design regarding user requirements.

	Multi-level topology	*CPU time*
Non-isolated dc-dc	3-level, $n_{cell(par)} = 2$	0.15 - 0.2 s
	5-level, $n_{cell(par)} = 4$	0.25 – 0.3 s
	7-level, $n_{cell(fc)} = 2$, $n_{cell(par)} = 3$	0.3 s
Three-phase inverter	2-level	2.7 - 4.4 s
	3-level, $n_{cell(fc)} = 2$	3.3 - 4.4 s
	3-level, $n_{cell(par)} = 2$	5.2 - 6 s

Table 8: CPU time to design different multilevel topologies

5.3. Loss comparison

Table 9 shows the comparison of semiconductor losses computed by Powerforge® and Plecs®. Differences are small enough to be considered negligible.

	Multi-level topology	*Losses in Powerforge*	*Losses in Plecs*
Non-isolated dc-dc	3-level, $n_{cell(par)} = 2$	137.2 W	136.16 W
	5-level, $n_{cell(par)} = 4$	181.5 W	181 W
	7-level, $n_{cell(fc)} = 2$, $n_{cell(par)} = 3$	219.3 W	219.25 W
Three-phase inverter	2-level	66.5 W	67.4 W
	3-level, $n_{cell(fc)} = 2$	109 W	107.6 W
	3-level, $n_{cell(par)} = 2$	49.8 W	53.4 W

Table 9: Comparison of semiconductor losses between Powerforge® and Plecs®

6. Conclusion

The principle of a frequency solver adapted to the commutation cell has been introduced. It allows power electronics designer to get steady-state waveforms much faster than a time-domain solver and harmonic spectrum is obtained with a very good accuracy.
At last, an application of this frequency solver to a computer-aided engineering platform dedicated to the design of power converters is presented. Some design examples have been proposed and show a very good compromise between the computation time and the accuracy of the losses which are computed in the semiconductors.

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